CLAIMS

What is claimed is:

1. An apparatus, comprising:

- an inductor capacitor (LC) tank;

- a drive circuit including a first generator, coupled to the LC tank, to drive the LC tank, and a current source, coupled to the first generator, to provide a source current to the first generator; and

- a feedback loop circuit including a peak detect circuit, coupled to the LC tank, to generate a peak detect voltage signal representing an oscillation amplitude of the LC tank; a reference voltage generator to generate a single reference voltage; and an operational amplifier, with a pair of input terminals coupled to the peak detect circuit and the reference voltage generator and an output terminal coupled to the current source, to generate an analog bias signal to adjust the magnitude of the current source.

2. The apparatus according to claim 1, wherein a capacitor is coupled between the output terminal of the operational amplifier and an electrical ground.

3. The apparatus according to claim 2, wherein the LC tank further comprises a first tank terminal and a second tank terminal; the first generator comprises a negative resistance generator including a first and a second drive transistor coupled to the first and second tank terminals; the first and second drive transistors have a pair of commonly coupled terminals; the current source is a single current source transistor coupled to the commonly coupled terminals to provide the source current to the first and second drive transistors; and the pair of input terminals of the peak detect circuit are coupled to the first and second tank terminals through a first and a second blocking capacitor.

4. The apparatus according to claim 3, wherein the peak detect circuit and the reference voltage generator include a plurality of identical components.

5. The apparatus according to claim 4, wherein the peak detect circuit includes:

- a first detect transistor coupled to the first tank terminal;

- a second detect transistor coupled to the second tank terminal and the first detect transistor, and

- a detect current source commonly coupled to the first and second detect transistors;

wherein the reference voltage circuit includes:

- a first reference transistor operable to receive a reference bias signal;

- a second reference transistor coupled the first reference transistor and operable to receive the reference bias signal, and

- a reference current source commonly coupled to the first and second reference transistors; and

wherein the first detect and first reference transistors are identical in design, the second detect and second reference transistors are identical in design, and the detect and reference current sources are identical in design.

6. The apparatus according to claim 5, wherein a gate of the first detect transistor is coupled to the first tank terminal and a gate of the second detect transistor is coupled to the second tank terminal; a drain of the first detect transistor and a drain of the second detect transistor are commonly coupled; a source of the first detect transistor and a source of the second detect transistor are commonly coupled; and the detect current source is coupled to the commonly coupled sources of the first and second detect transistors and wherein a gate of both the first and second reference transistors is operable to receive the reference bias signal; a drain of the first reference transistor and a drain of the second reference transistor are commonly coupled; a source of the first reference transistor; and a source of the second reference transistor are commonly coupled; and the reference current source is coupled to the commonly coupled sources of the first and second reference transistors.

7. The apparatus according to claim 6, wherein the LC tank has a first and a second LC resonator, the first LC resonator including a first inductance coupled between a supply voltage and the first tank terminal and a first variable capacitor coupled between the first tank terminal and a control node, the second LC resonator including a second inductance coupled between the supply voltage and the second tank terminal and a second variable capacitor coupled between the second tank terminal and the control node, the first drive transistor being coupled to the first tank terminal and cross-coupled the second tank terminal and the second drive transistor being coupled the second tank terminal and cross-coupled to the first tank terminal.

8. The apparatus according to claim 7, wherein the first drive transistor, the second drive transistor, and the current source transistor are MOSFETS; a drain of the first drive transistor is coupled to the first tank terminal; a gate of the first drive transistor is cross-coupled to the drain of the second tank terminal; a drain of the second drive transistor is coupled the second tank terminal; a gate of the second transistor is cross-coupled to the first tank terminal; a source of the first drive transistor and a source of the second drive transistor are commonly coupled to a drain of the current source transistor; a source of the current source transistor is coupled to ground; and a gate of the current source transistor is coupled to the output terminal of the operational amplifier to receive the analog bias signal.

9. The apparatus according to claim 8, wherein the operational amplifier is a folded cascode operational amplifier.

10. An apparatus, comprising:

- an inductor capacitor (LC) tank having a pair of tank terminals;
- a drive circuit including a first and a second drive transistor, coupled to the pair of tank terminals, having a pair of commonly coupled terminals and the single current source transistor, connected to the commonly coupled terminals, to provide a source current to the first and second drive transistors;

- a feedback loop circuit including a peak detect circuit, with a pair of input terminals coupled to the pair of tank terminals, to generate a peak detect voltage signal representative of an oscillation amplitude of the LC tank; a reference voltage generator to generate a single reference voltage; and an operational amplifier, with a pair of input terminals coupled to the peak detect circuit and the reference voltage generator and an output terminal coupled to the current source transistor, to generate an analog bias signal to adjust the magnitude of the source current.

11. The apparatus according to claim 10, wherein a compensation capacitor is coupled between the output terminal of the operational amplifier and an electrical ground.

12. The apparatus according to claim 10, wherein the pair of input terminals of the peak detect circuit are coupled to the first and second tank terminals through a first and a second blocking capacitor.

13. The apparatus according to claim 12, wherein the peak detect circuit and the reference voltage generator include a plurality of identical components.

14. The apparatus according to claim 12, wherein the peak detect circuit includes:

- a first detect transistor coupled to the first tank terminal;
- a second detect transistor coupled to the second tank terminal and the first detect transistor, and
- a detect current source commonly coupled to the first and second detect transistors;

wherein the reference voltage circuit includes:

- a first reference transistor operable to receive a reference bias signal;
- a second reference transistor coupled the first reference transistor and operable to receive the reference bias signal, and
- a reference current source commonly coupled to the first and second reference transistors; and

wherein the first detect and first reference transistors are identical in design, the second detect and second reference transistors are identical in design, and the detect and reference current sources are identical in design.

15. The apparatus according to claim 14, wherein a gate of the first detect transistor is coupled to the first tank terminal and a gate of the second detect transistor is coupled to the second tank terminal; a drain of the first detect transistor and a drain of the second detect transistor are commonly coupled; a source of the first detect transistor and a source of the second detect transistor are commonly coupled; and the detect current source is coupled to the commonly coupled sources of the first and second detect transistors and wherein a gate of both the first and second reference transistors is operable to receive the reference bias signal; a drain of the first reference transistor and a drain of the second reference transistor are commonly coupled; a source of the first reference transistor; and a source of the second reference transistor are commonly coupled; and the reference current source is coupled to the commonly coupled sources of the first and second reference transistors.

16. The apparatus according to claim 12, wherein the LC tank has a first and a second LC resonator, the first LC resonator including a first inductance coupled between a supply voltage and the first tank terminal and a first variable capacitor coupled between the first tank terminal and a control node, the second LC resonator including a second inductance coupled between the supply voltage and the second tank terminal and a second variable capacitor coupled between the second tank terminal and the control node, the first drive transistor being coupled to the first tank terminal and cross-coupled the second tank terminal and the second drive transistor being coupled the second tank terminal and cross-coupled to the first tank terminal.

17. The apparatus according to claim 16, wherein the first drive transistor, the second drive transistor, and the current source transistor are MOSFETS; a drain of the first drive transistor is coupled to the first tank terminal; a gate of the first drive transistor is cross-coupled to the drain of the second tank terminal; a drain of the second drive

transistor is coupled the second tank terminal; a gate of the second transistor is cross-coupled to the first tank terminal; a source of the first drive transistor and a source of the second drive transistor are commonly coupled to a drain of the current source transistor; a source of the current source transistor is coupled to ground; and a gate of the current source transistor is coupled to the output terminal of the operational amplifier to receive the analog bias signal.

18. The apparatus according to claim 12, wherein the operational amplifier is a folded cascode operational amplifier.

19. A system, comprising an integrated circuit having a receiver, the receiver having a phase lock loop (PLL) to recover a clock signal from a data signal; the PLL including a phase detector with a first input to receive the data signal; a loop filter having an input coupled to the output of the phase detector; and a voltage controlled oscillator (VCO) having an input coupled to the output of the loop filter and an output coupled to a second input of the phase detector; the VCO including an inductor capacitor (LC) tank; a drive circuit including a first generator, coupled to the LC tank, to drive the LC tank and a current source, coupled to the first generator, to provide a source current to the first generator; and a feedback loop circuit including a peak detect circuit, with a pair of input terminals coupled to the LC tank, to generate a peak detect voltage signal representing an oscillation amplitude of the LC tank; a reference voltage generator to generate a single reference voltage; and an operational amplifier, with a pair of input terminals coupled to the peak detect circuit and the reference voltage generator and an output terminal coupled to the current source transistor, to generate an analog bias signal to adjust the magnitude of the source current.

20. The system of claim 19, further comprising a fiber-optical data communications channel, coupled to the receiver, to provide the data signal to the receiver.

21. The system according to claim 19, wherein a capacitor is coupled between the output terminal of the operational amplifier and an electrical ground.

22. The system according to claim 19, wherein the LC tank has a first tank terminal and a second tank terminal; the first generator includes a negative resistance generator having a first and a second drive transistor coupled to the first and second tank terminals; the first and second drive transistors have a pair of commonly coupled terminals; the current source comprises a single current source transistor coupled to the commonly coupled terminals to provide the source current to the first and second drive transistors; and the pair of input terminals of the peak detect circuit are coupled to the first and second tank terminals through a first and a second blocking capacitor.

23. The system according to claim 22, wherein the peak detect circuit and the reference voltage generator include a plurality of identical components.

24. The system according to claim 23, wherein the peak detect circuit includes:

- a first detect transistor coupled to the first tank terminal;
- a second detect transistor coupled to the second tank terminal and the first detect transistor, and
- a detect current source commonly coupled to the first and second detect transistors;

wherein the reference voltage circuit includes:

- a first reference transistor operable to receive a reference bias signal;
- a second reference transistor coupled the first reference transistor and operable to receive the reference bias signal, and
- a reference current source commonly coupled to the first and second reference transistors; and

wherein the first detect and first reference transistors are identical in design, the second detect and second reference transistors are identical in design, and the detect and reference current sources are identical in design.

25. The system according to claim 24, wherein a gate of the first detect transistor is coupled to the first tank terminal and a gate of the second detect transistor is coupled to

the second tank terminal; a drain of the first detect transistor and a drain of the second detect transistor are commonly coupled; a source of the first detect transistor and a source of the second detect transistor are commonly coupled; and the detect current source is coupled to the commonly coupled sources of the first and second detect transistors and wherein a gate of both the first and second reference transistors is operable to receive the reference bias signal; a drain of the first reference transistor and a drain of the second reference transistor are commonly coupled; a source of the first reference transistor; and a source of the second reference transistor are commonly coupled; and the reference current source is coupled to the commonly coupled sources of the first and second reference transistors.

26. The system according to claim 25, wherein the LC tank has a first and a second LC resonator, the first LC resonator including a first inductance coupled between a supply voltage and the first tank terminal and a first variable capacitor coupled between the first tank terminal and a control node, the second LC resonator including a second inductance coupled between the supply voltage and the second tank terminal and a second variable capacitor coupled between the second tank terminal and the control node, the first drive transistor being coupled to the first tank terminal and cross-coupled the second tank terminal and the second drive transistor being coupled the second tank terminal and cross-coupled to the first tank terminal.

27. The system according to claim 26, wherein the first drive transistor, the second drive transistor, and the current source transistor are MOSFETS; a drain of the first drive transistor is coupled to the first tank terminal; a gate of the first drive transistor is cross-coupled to the drain of the second tank terminal; a drain of the second drive transistor is coupled the second tank terminal; a gate of the second transistor is cross-coupled to the first tank terminal; a source of the first drive transistor and a source of the second drive transistor are commonly coupled to a drain of the current source transistor; a source of the current source transistor is coupled to ground; and a gate of the current source transistor is coupled to the output terminal of the operational amplifier to receive the analog bias signal.

28. The system according to claim 27, wherein the operational amplifier is a folded cascode operational amplifier.